Cryo-CMOS Electronics for Scalable Quantum Computing

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A quantum computer comprises both a quantum processor cooled at cryogenic temperature and a classical electronic controller to operate and read out the quantum devices. Such controller is currently implemented at room temperature for the few qubits available today. However, due to the wiring requirements between the cryogenic quantum devices and room-temperature electronics, this approach becomes unfeasible as the number of qubits grows towards the tens of thousands required for quantum algorithms with practical applications. As an alternative, we propose a cryogenic electronic controller fabricated using CMOS technology, which is the only technology allowing the integration of the billions of transistors required to operate a very large number of qubits. This talk will address the challenges of building such CMOS controller, such as the modeling of cryo-CMOS devices for circuit simulation and design, and the co-simulation of the classical/quantum interface. By demonstrating the functionality of critical circuit components, including low-noise amplifiers for qubit read-out and signal generators for qubit control, we will conclude whether standard CMOS is a viable technology for the implementation of scalable electronic interfaces for quantum processors.